IN THE CLAIMS

1. (Currently amended) A power management system for dynamically managing power application to each of a plurality of devices in a computer system, ~~having one or more different components wherein power is dynamically supplied to each component,~~ the power management system comprising:

(a) a flexible clock generator circuit including at least one fixed rate clock signal oscillator, said generator circuit for generating one or more ~~different~~ clock signals, wherein the frequency of each of said signals can be in a range from less than to greater than the frequency of said fixed rate clock signal; and ~~wherein each clock signal has a different predetermined frequency~~;

(b) a clock selector circuit responsive to a rate of usage of each of said plurality of devices that directs a particular frequency of an output signal to be ~~that, based on the task being performed by the computer system, dynamically adjusts the clock signal~~ supplied to each of said plurality of devices to maintain operation of each of said plurality of devices and ~~each component of the computer system in order to reduce~~ minimize the total power being consumed by the computer system.

2. (Currently amended) The system of Claim 1 further comprising a static power management system ~~wherein power is withdrawn from components that are not currently active to reduce the power consumption of the computer system~~ for managing power application to each of said plurality of devices by withdrawing power from a device that is not currently active, and re-applying power when said device is needed to be active.

3. (Currently amended) The system of Claim 2, wherein the static power management system includes ~~further comprises~~ a circuit for disconnecting the address, and control data in and data out pins of a component of the computer system in order to reduce the power consumption of the computer system.

4. (Currently amended) The system of Claim 1, wherein the clock generator circuit includes ~~further comprises~~ a first oscillator that generates a first clock signal, a second clock oscillator that generates a second clock signal, and a programmable clock circuit that generates a third clock signal based on the second clock signal, ~~and a~~ wherein said clock select circuit ~~that~~ selects one of the first, second and third clock ~~signal~~ signals that is supplied to a portion of the computer system to provide that portion of the computer system with a predetermined clock signal.

5. (Currently amended) The system of Claim 4, wherein the clock select circuit includes ~~further comprises~~ a clock state machine for determining the clock state of the computer system at a predetermined time and a clock policy circuit for generating control signals to the clock select circuit in order to output the appropriate clock signal.

6. (Currently amended) The system of Claim 5, wherein the clock state machine provides ~~further comprises~~ an idle state ~~wherein~~ when the computer system is waiting for an input, a busy state ~~wherein~~ when the computer system is performing a task, a sleep state ~~wherein~~ when the computer system has timed out due to inactivity and a dead state ~~wherein~~ when power has failed to the computer system.

7. (Currently amended) The system of Claim 6, wherein the clock select circuit includes ~~further comprises~~ a circuit that generates a system clock, a circuit that generates a processor clock and a circuit that generates a co-processor clock wherein each of the clocks is independently and simultaneously operable.

8. (Currently amended) The system of Claim 6, wherein, during the idle state~~,~~ the clock select circuit generates no clock for the phase locked loop and co-processor so that they are off, the clock select circuit generates the first clock signal for the processor so that the processor is clocked at a slow rate and the clock select circuit generates a high rate clock for an interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the computer system ~~quickly~~.

9. (Original) The system of Claim 6, wherein, during the busy state, the clock select circuit generates a high rate clock signal for the processor, the co-processor and the interrupt circuits.

10. (Original) The system of Claim 6, wherein, during the sleep state, the clock select circuit generates no clock signal for the processor and the co-processor.

11. (Original) The system of Claim 5, wherein the clock state machine is controlled by an interrupt signal and software commands.

12. (Original) The system of Claim 4, wherein the programmable clock circuit generates a fourth clock signal.

13. (Original) The system of Claim 12, wherein the first, second, third and fourth clock signals have different frequencies.

14. (Currently amended) The system of Claim 13, wherein the first clock signal frequency is ~~comprises~~ 32 kHz, the second clock signal frequency ~~comprises~~ is 24 MhZ, the third clock signal frequency ~~comprises~~ is 33 MhZ and the fourth clock signal frequency ~~comprises~~ is 66 MhZ.

15. (Currently amended) The system of Claim 4 further ~~comprises~~ comprising a time of day circuit that generates time of day clock signals based on the first clock signal.

16. (Currently amended) The system of Claim 4, wherein the clock select circuit ~~further comprises~~ includes means for dynamically changing the clock frequency applied to each device ~~component~~ of the computer system based on the task being performed by the computer system.

17. (Currently amended) The system of Claim 4, wherein the clock select circuit ~~comprises~~ includes a multiplexer.

18. (Currently amended) The system of Claim 4, wherein the programmable clock generator further ~~comprises~~ includes a prescalar unit and a post scalar unit whose outputs are fed into a phase locked loop that generates a third clock signal and a fourth clock signal having different frequencies.

19. (Currently amended) A power management method for a computer system having ~~one or more different components~~ a plurality of devices wherein power is dynamically supplied to each device ~~component~~, the power management method comprising:

(a) ~~simultaneously~~ generating by a clock generator having a crystal oscillator one or more different clock signals wherein each clock signal has a different predetermined frequency, and wherein said predetermined frequencies are selectable in a frequency range from less than to greater than a frequency of said crystal oscillator; and

(b) dynamically ~~adjusts~~ adjusting the clock signal supplied to each ~~component,~~ device of the computer system in order to reduce the total power being consumed by the computer system.

20. (Currently amended) The method of Claim 19 further comprising ~~static power management method wherein power is withdrawn~~ withdrawing power from ~~components~~ devices that are not currently active to reduce the power consumption of the computer system so as to provide static power management ~~method~~.

21. (Currently amended) The method of Claim 20, wherein said withdrawing power includes ~~the static power management further comprises~~ disconnecting ~~the~~ an address, and control data in and data out pins of a ~~component~~ device of the computer system ~~method~~ in order to reduce the power consumption of the computer system ~~method~~.

22. (Currently amended) The method of Claim 19, wherein ~~the clock generation further comprises~~ said generating further includes generating a first clock signal with a first oscillator, generating a second clock signal using a second oscillator, generating a third clock

signal based on the second clock ~~signal~~ signals, and selecting by a programmable clock select circuit one of the first, second and third clock signals that is supplied to a portion of the computer system to provide that portion of the computer system with a predetermined clock signal.

23. (Currently amended) The method of Claim 22, wherein ~~the clock select further comprises~~ said selecting further includes determining by a state machine the clock state of the computer system at a predetermined time and generating control signals to the clock select circuit in order to output the appropriate clock signal.

24. (Currently amended) The method of Claim 23, wherein said selecting further includes ~~the clock state machine further comprises~~ an idle state wherein the computer system ~~method~~ is waiting for an input, a busy state wherein the computer system ~~method~~ is performing a task, a sleep state wherein the computer system has timed out due to inactivity and a dead state wherein power has failed to the computer system.

25. (Currently amended) The method of Claim 24, wherein said selecting further includes ~~the clock select circuit further comprises~~ generating a system clock, generating a processor clock and generating a co-processor clock wherein each of the clocks is independently and simultaneously operable.

26. (Currently amended) The method of Claim 24, wherein during the idle state, ~~generating~~ no clock signal is provided to ~~for~~ the phase locked loop and co-processor so that they are off, and generating the first clock signal for the processor so that the processor is clocked at a slow rate and generating a high rate clock for an interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the computer system ~~method quickly~~.

27. (Currently amended) The method of Claim 24, wherein during the busy state, ~~generating~~ a high rate clock signal is applied to ~~for~~ the processor, the co-processor and the interrupt circuits.

28. (Currently amended) The method of Claim 24, wherein during the sleep state, ~~generating~~ no clock signal is applied to ~~for~~ the processor and the co-processor.

29. (Original) The method of Claim 23, wherein the clock state machine is controlled by an interrupt signal and software commands.

30. (Original) The method of Claim 22 further comprising generating a fourth clock signal.

31. (Original) The method of Claim 30, wherein the first, second, third and fourth clock signals have different frequencies.

32. (Currently amended) The method of Claim 31, wherein the first clock signal frequency ~~comprises~~ is 32 kHz, the second clock signal frequency ~~comprises~~ is 24 MhZ, the third clock signal frequency ~~comprises~~ is 33 MhZ and the fourth clock signal frequency ~~comprises~~ is 66 MhZ.

33. (Currently amended) The method of Claim 22 further comprising generating ~~comprises a time of day circuit that generates~~ time of day clock signals based on the first clock signal.

34. (Currently amended) The method of Claim 22, wherein the clock select circuit further ~~comprises~~ includes means for dynamically changing the clock frequency applied to each device ~~component~~ of the computer system ~~method~~ based on the task being performed by the computer system ~~method~~.

35. (Currently amended) The method of Claim 22, wherein the clock select circuit ~~comprises~~ includes a multiplexer.

36. (Currently amended) The method of Claim 22, wherein the programmable clock circuit ~~method~~ further includes ~~comprises~~ a prescalar unit and a post scalar unit ~~whose~~ having outputs that are fed into a phase locked loop that generates a third clock signal and a fourth clock signal having different frequencies.

37. (Currently amended) A flexible clock generator, comprising:

a first oscillator that generates a first clock signal;

a second clock oscillator that generates a second clock signal;

a programmable clock circuit that generates a third clock signal based on the second clock signal wherein a frequency of said third clock signal can be in a range from less than to greater than a frequency of said second clock signal; and

a clock select circuit that selects one of the first, second and third clock signals ~~signal~~ that is supplied to a portion of the computer system to provide that portion of the computer system with a predetermined clock signal.

38. (Currently amended) The generator of Claim 37, wherein the clock select circuit ~~further comprises~~ includes a clock state machine for determining the clock state of the computer system at a predetermined time and a clock policy circuit for generating control signals to the clock select circuit in order to output the appropriate clock signal.

39. (Currently amended) The generator of Claim 38, wherein the clock state machine ~~further comprises~~ provides an idle state wherein the computer system is waiting for an input, a busy state wherein the computer system is performing a task, a sleep state wherein the computer system has timed out due to inactivity and a dead state wherein power has failed to the computer system.

40. (Currently amended) The generator of Claim 39, wherein the clock select circuit further ~~comprises~~ includes a circuit that generates a system clock, a circuit that generates a processor clock and a circuit that generates a co-processor clock wherein each of the clocks is independently and simultaneously operable.

41. (Currently amended) The generator of Claim 39, wherein, during the idle state, the clock select circuit generates no clock for the phase locked loop and co-processor so that they are off, the clock select circuit generates the first clock signal for the processor so that the processor is clocked at a slow rate and the clock select circuit generates a high rate clock for an interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the computer system ~~quickly~~.

42. (Original) The generator of Claim 39, wherein, during the busy state, the clock select circuit generates a high rate clock signal for the processor, the co-processor and the interrupt circuits.

43. (Original) The generator of Claim 39, wherein, during the sleep state, the clock select circuit generates no clock signal for the processor and the co-processor.

44. (Original) The generator of Claim 38, wherein the clock state machine is controlled by an interrupt signal and software commands.

45. (Original) The generator of Claim 37, wherein the programmable clock circuit generates a fourth clock signal.

46. (Original) The generator of Claim 45, wherein the first, second, third and fourth clock signals have different frequencies.

47. (Currently amended) The generator of Claim 46, wherein a frequency of the first clock signal ~~frequency comprises~~ is 32 kHz, a frequency of the second clock signal ~~frequency comprises~~ is 24 MhZ, a frequency of the third clock signal ~~frequency comprises~~ is 33 MhZ and a frequency of the fourth clock signal ~~frequency comprises~~ is 66 MhZ.

48. (Currently amended) The generator of Claim 37 further ~~comprises~~ comprising a time of day circuit that generates time of day clock signals based on the first clock signal.

49. (Currently amended) The generator of Claim 37, wherein the clock select circuit ~~further comprises~~ includes means for dynamically changing the clock frequency applied to each component of the computer system based on ~~the~~ a task being performed by the computer system.

50. (Currently amended) The generator of Claim 37, wherein the clock select circuit ~~comprises~~ includes a multiplexer.

51. (Currently amended) The generator of Claim 37, wherein the programmable clock generator ~~further comprises~~ includes a prescalar unit and a post scalar unit whose outputs are fed into a phase locked loop that generates a third clock signal and a fourth clock signal having different frequencies.

52. (New) A power management method for a computer system comprising:

dynamically managing power application to each of a plurality of devices of said computer system including

a) first sensing a current operational usage of each said device; and

b) adjusting a frequency of a clock signal from a clock generator to each said device, said frequency in proportion to said usage, wherein said clock signal is supplied by a flexible clock generator including at least one oscillator, and wherein said generator can output at least one signal having a frequency adjustable from less than to greater than a frequency of said at least one oscillator.

53. (New) The method of Claim 52, further comprising:

statically managing power application to each said device including

a) second sensing to determine if a system device is being used;

b) withdrawing power including a clock signal from a device, if said device is not being used;

c) determining if an unpowered device is needed; and

d) applying power including a clock signal to said unpowered device if said device is needed.

54. (New) The method of Claim 53 further comprising:

optimizing by a device controller to manage said dynamic power application to each device for a lowest computer system power consumption consistent with required operation of each said device.

55. (New) The method of Claim 53 wherein said withdrawing power includes gating off logic and a clock signal to a device, and applying power includes reapplying logic and a clock signal to said device.